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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/984,562	12/03/97	MAILLOUX J	95-0653.02

LM02/1030

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EXAMINER	
KIM, H	

ART UNIT	PAPER NUMBER
2751	24

DATE MAILED: 10/30/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

☆U.S.GOVERNMENT PRINTING OFFICE 1995-319-826

Office Action Summary

Application No.	Applicant(s)
08/984,562	Mailloux et al.
Examiner	Group Art Unit

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 12/3/97 + 5/7/98.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 22-32 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 22-32 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other_____

Office Action Summary

Detailed Action

1. Claims 22-32 are presented for examination. This office action is in response to the Amendment filed on 12/03/97.

2. Receipt is acknowledged of Petition for Corrected Filing Receipt statement filed on 5/7/98, which statement has been placed of record in the file.

3. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

4. It is noted that this application appears to claim subject matter disclosed in the co-pending section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending applications to avoid possible double patenting.

5. The status of the related U.S. applications or patents should be included as appropriate in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification, if any. (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.)

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature.

It appears --selecting between burst and pipeline -- should be included in the title so that the title is more descriptive of the claimed invention.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 22-27 are rejected under 35 USC § 103(a) as being unpatentable over S3 Incorporated, S3 Burst Mode DRAM, 6/93 in view of *Johnson et al.*, (Johnson) U.S. Patent 4,581,990 or *Manning*, U.S. Patent 5,610,864.

As to claim 22, *S3 Incorp.*, discloses a memory circuit comprising; temporary circuit for

receiving a first external address (Figs. 3 & 4 Row address) and a multiplexer coupled to the storage (page 1 left column); mode selection by the memory controller (page 1, left column in the introduction section). However S3 Incorp. does not specifically mode control logic is in the memory.

It is well known in the art to combine the mode control logic and the memory circuit into one chip to take advantage of increasing the speed and decreasing the size and line noise between two units thereby increasing the overall system throughput and performance. See In re Larson, 144 USPQ 347 (CCPA 1965) and In re Lockhart, 90 USPQ 214 (CCPA 1951).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate mode control logic into the invention of S3 Incorp. because it would increase memory data throughput by decreasing the size and line noise between two units thereby more supportive in the market place. However S3 Incorp. does not specifically disclose a pipeline mode.

Johnson discloses inventive concept of selecting between a bust mode and a pipeline mode of operation (Figs. 5 and 6 & col. 10 lines 48-49) for the purpose of increasing memory data throughput in a system by a parallel and overlapping processing. Alternatively, *Manning* discloses a mode circuitry configure to select between two modes (Fig. 1 Ref. 40 & col. 5 lines 41- 50 and col. 6 lines 14-16) for the purpose of providing versatility thereby improving data throughput. It is highly desirable in a storage device to support the pipeline mode over the page mode because it would improve data throughput and versatility of the memory.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace a page mode of S3 Incorp. with a pipeline mode of *Johnson or Manning* because it would increase memory data throughput by parallel and overlapping processing and provide versatility of the memory by supporting latest technology in the market.

As to claims 23 and 24, S3 Incorp. further discloses external mode select signal and enable signal (page 1, left column in the introduction section).

As to claim 25, S3 Incorp. further discloses write enable and output enable (page 1 left column).

As to claim 26, S3 Incorp. further discloses a counter (page 1 left column).

As to claim 27, S3 Incorp. further discloses the counter is used in the burst mode (page 1 left column).

9. Claims 28-32 are rejected under 35 USC § 103(a) as being unpatentable over S3 Incorporated, S3 Burst Mode DRAM, 6/93, 2 pages in view of *Johnson et al.*, (Johnson) U.S. Patent 4,581,990 or *Manning*, U.S. Patent 5,610,864 and further in view of Micron Technology Inc., "1995 DRAM Data Book", page 4-1 through 4-42.

As to claim 28, *S3 Incorp., Johnson, and Manning* disclose the invention as claimed in the above claims but neither *S3 Incorp., Johnson, nor Manning* disclose a step of obtaining a second external address subsequent to the first external address in the pipe line mode. However, it was well known in the art that the step of obtaining a second external address subsequent to the first external address in the pipe line mode (page 4-2, left upper column) for the purpose of achieving high speed fully random access of the memory (page 4-2, left upper column) as shown by Micron. It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known concept of obtaining a second external address subsequent to the first external address in the pipe line mode of Micron into the combined invention of *S3 Incorp., Johnson, and Manning* because Micron states that it would achieve high speed fully random access of the memory.

As to claim 29, S3 Incorp. further discloses EDO modes (page 1).

As to claims 30 and 31, Micron further discloses CAS delay latency during a write and read cycle (page 4-6 and 4-7).

As to claim 32, Johnson further discloses a system clock coupled to the processor (Fig. 2,

SYSCLK), the memory not operating directly off the system clock ("If not, a simple access is completed with result and *IRDY or *DRDY being driven over the interface by the slave device. The processor latched the result, and the simple access is complete" (col. 10 lines 50-54) reads on this limitation because it indicates Asynchrous memory operation).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. USP 5,652,724, Jul. 29, 1997, Burst EDO memory device having pipelined output buffer; Troy A. Manning.
2. USP 5,610,864, Mar. 11, 1997, Burst EDO memory device with maximized write cycle timing; Troy A. Manning.
3. USP 5,526,320, Jun. 11, 1996, Burst EDO memory device; Paul S. Zagar, et al..
4. USP 5,392,239, Feb. 21, 1995, Burst-mode DRAM; Neal D. Margulis, et al.
5. USP 5,175,835, Dec. 29, 1992, Multi-mode DRAM controller; Edward W. Beighe, et al..
6. USP 5,146,582, Sep. 8, 1992, Data processing system with means to convert burst operations into memory pipelined operations; Ralph M. Begun.
7. USP 4,851,990, Jul. 25, 1989, High performance processor interface between a single chip processor and off chip memory means having a dedicated and shared bus structure; William M. Johnson, et al..
8. USP 4,519,028, May 21, 1985, CPU with multi-stage mode register for defining CPU operating environment including charging its communications protocol; Richard E. Olsen, et al..

9. Micron Technology Inc., "1995 DRAM Data Book", pp 4-1 through 4-42, 12/95.
10. S3 Incorporated, "S3 Burst Mode DRAM", 2 pages, 6/93.
11. Oki Electric Ind. Co., Ltd., "Burst DRAM Function & Pinout", JC42.3 Albuquerque, 2nd Presentation, 4 pages, Sept., 1994.

11. A shortened statutory period for response to this action is set to expire 3 (three) months

and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

13. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

14. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

15. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

17. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051-2, (for formal communications intended for entry)

Or:

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Patent Examiner
October 26, 1998

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER